IN THE UNITED STATES PATENT AND TRADEMARK OFFICE — PATENT APPLICATION

PCT #

Inventor(s): HIROSE et al.
Appln. No.: 09 / 787,321 (Series Code / Serial No.)
Filed: May 17, 2001

Group Art Unit: Unassigned
Examiner: Unassigned
Atty. Dkt. P 276725 / 7031P-U (M# / Client Ref)
Appln. Title: Multi-Layer Build-Up Wiring Board

JC05 Rec'd PCT/PTO 20 JUL 2001

OIPE JC177 JUL 20 2001 PATENT & TRADEMARK OFFICE

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Hon. Commissioner of Patents
Washington, D.C. 20231

Sir:

Date: July 20, 2001

REPLY/AMENDMENT/LETTER

This is a reply/amendment/letter in the above-identified application and includes the herewith attachment of same date and subject which is incorporated hereinto by reference and the signature below is treated as the signature to the attachment in absence of a signature thereto.

FEE REQUIREMENTS FOR CLAIMS AS AMENDED

1. Small Entity claim
A. ☐ NOT made
B. ☐ Withdrawn
C. ☐ made herewith
D. ☐ made previously
(For B & C See Required Separate Paper (Pat-256))

	Claims remaining after amendment	Highest number previously paid for		Present Extra	Large/Small Entity	Additional Fee	Fee Code Lg/Sm
2. Total Effective Claims	14	**minus	20	0	x $18/$9 =	+ $0	103/203
3. Independent Claims	13	***minus	3	10	x $80/$40 =	+ $800	102/202
4. If amendment enters proper multiple dependent claim(s) into this application for first time (leave blank if this is a reissue application) ..... add					+ $270/$135 =	+ $0	104/204
5. Original due Date: ☒ NONE							
6. Petition is hereby made to extend the original due date to cover the date this response is filed for which the requisite fee is attached (1 mo) (2 mos) (3 mos) (Usable only for ≤ 2mo.OA - - - 4 mos) (Usable only for 30 day/1mo.OA - - - 5 mos)				$110/$55 = $390/$195 = $890/$445 = $1390/$695= $1890/$945=	+ $0		115/215 116/216 117/217 118/218 128/228
7. Enter any previous extension fee paid since above original due date and subtract					- $0		
8.					Extension Fee Attached	+ $0	
9. If Terminal Disclaimer attached, add Rule 20(d) official fee					+ $110/$55	+ $0	148/248
10. If IDS attached requires Official Fee under Rule 97 (c), ... add or if Rule 97(d) Request ..... add					+ $180 + $180	+ $0	126 126
11. After-Final Request Fee per rules 129(a) and 17(r)					+ $710/355	+ $0	146/246
12. No. of additional inventions for examination per Rule 129(b).....					x $710/355 ea	+ $0	149/249
13. Request for Continued Examination (RCE)					+ $710/355	+ $0	1179/1279
14. Petition fee for						+ $0	
15.					TOTAL FEE ENCLOSED =	$800	

16. *If the entry in this space is less than entry in next space, the "Present Extra" result is "0".
17. **If the "Highest number previously paid for" in this space is less than 20, write "20" in this space.
18. ***If the "Highest number previously paid for" in this space is less than 3, write "3" in this space.

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Our Deposit Account No. 03-3975)
(Our Order No. 41226 (C#) / 276725 (M#))

CHARGE STATEMENT: The Commissioner is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fee(s) filed, or asserted to be filed, or which should have been filed herewith or concerning any paper filed hereafter, and which may be required under Rules 16-18 (missing or insufficiencies only) now or hereafter relative to this application and the resulting Official Document under Rule 20, or credit any overpayment, to our Accounting/Order Nos. shown above, for which purpose a duplicate copy of this sheet is attached.
This CHARGE STATEMENT does not authorize charge of the issue fee until/unless an issue fee transmittal sheet is filed.

Query: Is appeal deadline now? If so, file Notice of Appeals separately.

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NOTE: File this cover sheet in duplicate with PTO receipt (PAT-103A) and attachments

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Pre Amdt B

Rabbed 11/9/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION OF

HIROSE et al

Appln. No.: 09/787,321

Filed: March 16, 2001

Title: MULTI-LAYER BUILD-UP WIRING BOARD

Group Art Unit: Unassigned

Examiner: Unassigned

July 20, 2001

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PRELIMINARY AMENDMENT

Hon. Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-identified patent application, please enter the following amendments.

IN THE CLAIMS:

Please enter the following amended claims:

1. (Amended) A multilayer build-up wiring board obtained by alternately providing interlayer resin insulating layers and conductor layers comprising:

a plurality of plain layers formed as said conductor layers; and

mesh holes formed in said plurality of plain layers so that at least part of the mesh holes overlay one another.

2. (Amended) A multilayer build-up wiring board obtained by alternately providing interlayer resin insulating layers and conductor layers, comprising:

a plain layer serving as a conductor layer formed on one side of said core substrate;

a plain layer formed out of at least one of the conductor layers formed between said interlayer resin insulating layers; and

mesh holes formed in the plain layer of said core substrate and the plain layer between said interlayer resin insulating layers so that at least part of the mesh holes overlay one another.

3. (Amended) The multilayer build-up wiring board of claim 1, wherein a diameter of each of said mesh holes is set at 75 to 300 μm and a distance between the mesh holes is set at 100 to 1500 μm

4. (Amended) A multilayer build-up wiring board obtained by alternately providing interlayer resin insulating layers and conductor layers, provided with a chip mount region on which a chip is mounted on an outermost layer and having the conductor layers connected to each other by via holes, respectively comprising:

mesh holes provided in plain layers formed as said conductor layers; and

lands of through holes or the via holes provided in at least part of the mesh holes in a region facing said chip mount region through the interlayer resin insulating layers.

5. (Amended) A multilayer build-up wiring board obtained by alternately providing interlayer resin insulating layers and conductor layers, provided with a chip mount region on an outermost layer and having the conductor layer connected to each other by via holes, respectively, comprising:

mesh holes provided in plain layers formed as said conductor layers; and

lands of the via holes provided in at least part of the mesh holes in a region facing said chip mount region through the interlayer resin insulating layers.

6. (Amended) A multilayer build-up wiring board obtained by alternately providing interlayer resin insulating layers and conductor layers, provided with a chip mount region on an outermost layer comprising:

mesh holes provided in plain layers formed as said conductor layers; and

solid conductor layers provided in at least part of the mesh holes in a region facing said chip mount region through the interlayer resin insulating layers.

7. (Amended) A multilayer build-up wiring board wherein interlayer resin insulating layers and conductor layers are alternately provided on a substrate having through holes and a chip mount region for mounting a chip provided on an outermost layer, comprising:

mesh holes provided in plain layers formed as said conductor layers; and

lands of the through holes provided in at least part of the mesh holes in a region facing said chip mount region through the interlayer resin insulating layers.

8. (Amended) A multilayer build-up wiring board having a multilayer wiring layer, wherein interlayer resin insulating layers and conductor layers are alternately provided and the conductor layers are connected to each other by via holes, respectively, the multilayer wiring layer formed on a core substrate, wherein one of said via holes is formed out of a plurality of wiring paths.

9. (amended) A multilayer build-up wiring board having a multilayer wiring layer, wherein the interlayer resin insulating layer and conductor layer are alternately provided and the conductor layers are connected to each other by via holes, respectively, the multilayer wiring layer formed on a core substrate wherein, one of said via holes is formed out of two wiring paths.

10. (Amended) A multilayer build-up wiring board having a multilayer wiring layer, wherein interlayer resin insulating layers and conductor layers are alternately provided and the conductor layers are connected to each other by via holes, respectively, the multilayer wiring layer formed on a core substrate, said conductor layers electrically connected to conductor layers on a back side of the core substrate by through holes formed in the core substrate, respectively comprising:

a plurality of wiring paths provided in each of the through holes in said core substrate; and

via holes consisting of a plurality of wiring paths each connected to each of said wiring paths of said through holes provided right on said through holes in which said plurality of wiring paths are provided.

11. (Amended) A multilayer build-up wiring board having a multilayer wiring layer, wherein interlayer resin insulating layers and conductor layers are alternately provided and the conductor layers are connected to each other by via holes, the multilayer wiring layer formed on both sides of a core substrate, conductor layers of the both sides of said core substrate electrically connected to one another by through holes formed in the core substrate, comprising:

a plurality of wiring paths provided in each of the through holes in said core substrate; and

via holes consisting of a plurality of wiring paths each connected to each of said wiring paths of said through hole provided right on said through holes in which said plurality of wiring paths are provided.

12. (Amended) A multilayer build-up wiring board having a multilayer wiring layer, wherein interlayer resin insulating layers and conductor layers are alternately provided and the conductor layers are connected to each other by via holes, the multilayer wiring layer formed on both sides of a core substrate electrically connected to one another by through holes formed in the core substrate, comprising:

a filler filled in the through holes of said core substrate and a conductor layer covering an exposed surface of the filler from the through holes formed in the through hole; the through holes and the conductor layers divided into a plurality of parts, respectively; and

via holes consisting of wiring paths connected to the divided parts of the conductor layers, respectively, provided right on the through holes covered with said divided parts of the conductor layers.

13. (Amended) A wiring board having a conductor circuit including a conductor layer of two-layer structure in which a second metal film thinner than a first metal film is provided on said first metal film, comprising:

sides of the second metal film forming said conductor layer protruding farther outside said conductor layer than said first metal film,

resin insulating layers provided on the conductor layers.

14. (Amended) A multilayer build-up wiring board having a structure in which at least one resin insulating layer and at least one conductor circuit is formed on a resin substrate, comprising:

at least one layer of said conductor circuit including a conductor layer of a two layer structure in which a second metal film thinner than a first metal film is provided on said first metal film; and

sides of the second metal film forming said conductor layer protruding farther outside said conductor layer than said first metal film.

See the attached Appendix for the changes made to effect the above claims

REMARKS

Applicants respectfully submit that no new matter is added by this Preliminary Amendment.

Attached hereto is a marked-up version of the changes made to the claims by the current Preliminary Amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

It is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

Pillsbury Winthrop LLP

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Enclosure: Appendix